

REMARKS

Claim 12 is amended; and as a result, claims 1-16 are pending in the above-identified patent application.

§102 Rejection of the Claims

Claims 1-16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Morrison *et al.* (U.S. 6,601,165). Applicant does not admit that Morrison *et al.* is prior art and reserves the right, as provided for under 37 C.F.R. 1.131, to "swear behind" Morrison *et al.* Applicant respectfully traverses the rejection of claims 1-16.

Claim 1 recites, "testing the bootstrap processor to verify that it will run BIOS code." In contrast, Morrison *et al.* in the abstract states, "The apparatus attempts a cold reset of the system, during which each processor performs a built-in self test." Thus, it appears that Morrison *et al.* fails to teach "testing the bootstrap processor to verify that it will run BIOS code." Further, the Office action fails to cite to columns or lines in Morrison *et al.* that teach "testing the bootstrap processor to verify that it will run BIOS code." In addition, applicant's representative has studied Morrison *et al.* and it appears to applicant's representative that Morrison *et al.* does not teach "testing the bootstrap processor to verify that it will run BIOS code." Thus, Morrison *et al.* fails to teach each of the elements of claim 1. Hence the Office action fails to state a *prima facie* case of anticipation with respect to claim 1. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 1.

Claims 2-5 are dependent on claim 1. For reasons analogous to those stated above and elements in the claims, applicant respectfully submits that the Office action fails to state a *prima facie* case of anticipation with respect to claims 2-5. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 2-5.

Claims 6 and 12 recite, "a latch for turning off said bootstrap processor." The Office action, in paragraph 3 cites to the abstract and column 1, line 44, through column 2, line 15, as teaching "a latch for turning off said bootstrap processor." Applicant's representative has studied Morrison *et al.* including the abstract and column 1, line 44, through column 2, line 15, and respectfully submits that Morrison *et al.* does not teach "a latch for turning off said bootstrap processor," as recited in claims 6 and 12. And with respect to bootstrap processors, Morrison *et*

al., in the abstract, teaches, "The apparatus selects a boot strap processor to perform a warm reset, during which an failed processors are tristated using a flush command." And with respect to bootstrap processors, at column 1, lines 65-67, and column 2, lines 1-2, Morrison *et al.* teaches; "The method further includes attempting to identify one of the node-boot strap processors as a system boot-strap processor and using the system-boot strap processor to perform a warm reset of the plurality of processors in each of the nodes." Thus, although Morrison *et al.* references bootstrap processors, Morrison *et al.* fails to teach "a latch for turning off said bootstrap processor." Hence, Office action fails to state a *prima facie* case of anticipation with respect to claims 6 and 12. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 6 and 12.

Claims 7-11 are dependent on claim 6. Claims 13-16 are dependent on claim 12. For reasons analogous to those stated above and elements in the claims, applicant respectfully submits that the Office action fails to state a *prima facie* case of anticipation with respect to claims 7-11 and claims 13-16. Therefore, applicant requests withdrawal of the rejections and reconsideration and allowance of claims 7-11 and 13-16.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 09/883,386

Filing Date: June 19, 2001

Title: FAULT RESILIENT BOOTING FOR MULTIPROCESSOR SYSTEM USING APPLIANCE SERVER MANAGEMENT

Assignee: Intel Corporation

Page 7

Dkt: 884.923US1 (INTEL)

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone applicant's attorney at 612-371-2109 to facilitate prosecution of the above-identified patent application.

If necessary, please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SON H. LAM

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Attorneys for Intel Corporation

P.O. Box 2938

Minneapolis, Minnesota 55402

612-371-2109

Date

July 6, 2004

By

Danny J. Pady

Reg. No. 35,635

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 6 day of July, 2004.

ANNE M. RICHARDS

Name

Signature

Anne M. Richards